We Claim:

1. A test system for testing a first memory circuit and a second memory circuit in parallel, the test system comprising:

a tester unit configured to generate a circuit select signal for activating the first and second memory circuits to receive signals in dependence on the circuit select signal;

the first memory circuit and the second memory circuit each having a test data generator circuit for generating test data for writing to memory cells of the respective memory circuit; and

wherein the first memory circuit and the second memory circuit are connected to said tester unit in such a way as to simultaneously apply the circuit select signal to the first memory circuit in inverted form and to the second memory circuit in noninverted form.

2. The test system according to claim 1, which comprises an inverter unit connected between the first memory circuit and said tester unit.

3. The test system according to claim 1, connected to and configured to test a plurality of first memory circuits and/or a plurality of second memory circuit.

4. The test system according to claim 1, wherein at least one of the first and second memory circuits is a DRAM memory circuit.

5. A method for testing a first and a second memory circuit, which comprises:

providing first and second memory circuits each configured to be activated in dependence on a circuit select signal;

enabling the first and second memory circuits to receive a control signal, the control signal initiating a function in the respective memory circuit depending on an activation of the first or second memory circuit;

for testing the memory circuits, applying the circuit select signal to the first memory circuit and applying the circuit select signal in inverted form to the second memory circuit, for initiating the function in the first or in the second memory circuit depending on the circuit select signal.

6. The method according to claim 5, which comprises applying the control signal to a signal input of the respective memory circuit.

7. The method according to claim 5, which comprises setting the circuit select signal to a first state for activating the first memory circuit and deactivating the second memory circuit, and setting the circuit select signal to a second state for activating the second memory circuit and deactivating the first memory circuit in the second state.

8. The method according to claim 5, wherein the control signal is at least one signal selected from the group consisting of a RAS signal, a CAS signal, and a WE signal.